UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,345	12/29/2003	Mark L. Doczy	42P17820	8139

8791 7590 06/05/2006

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
THAI, LUAN C	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,345	DOCZY ET AL.	
	Examiner	Art Unit	
	Luan Thai	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-8 and 10-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-8 and 10-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-2, 4-5, 7-8, and 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (6,040,224 of record) in view of Chau et al. (6,890,807 of record).

Regarding claims 1, 4-5, 7, 10, and 16, Tsukamoto (see specifically figure 5C-5E) disclose a method of forming a microelectronic structure comprising: providing a substrate (11) comprising source/drain regions (21) and gate region (18), wherein the gate region comprises a metal layer (15) of tungsten disposed on a gate dielectric layer (13) of silicon dioxide, a polysilicon layer (16) disposed on the metal layer (15), laser annealing the substrate to activate the implanted species (Col. 4, lines 65+). Since the doped polysilicon film (16) is adapted to protect the metal gate layer (15) from the laser annealing (Col. 4, lines 25+), the metal gate layer (15) is considered *"not substantially diffuse into the gate dielectric layer"*. Tsukamoto fails to teach the gate dielectric layer (13) being a high-k dielectric layer.

Chau et al. while related to a similar method of forming a microelectronic structure teach that the silicon dioxide, which is used to form the gate dielectric layer, being replaced by a high-k dielectric layer (Col. 1, lines 13+), such as hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide (Col. 2, lines 32+), in order to reduce gate leakage (Col. 1, lines 14+). It would have been obvious to a person of ordinary skill in the art at the time the invention was

made to recognize that combining Chau et la.'s teaching with Tsukamoto's invention would have been beneficial because it helps to reduce gate leakage.

Regarding claims 11 and 14, Tsukamoto teaches the metal layer (15) made of tungsten, wherein tungsten is inherent to have a work function about 4eV, as evidenced by Bustos et al. (U.S. 2004/0126977, paragraph [0067]); and thus, the work function of tungsten layer (15) is approximately equal to the work function of a doped polysilicon, as evidenced by Applicant's Specification, paragraph [0018].

Regarding claims 8 and 12, Tsukamoto's figures 5D-5E show the ratio of the depth of the source/drain regions (21) to the length of the source/drain regions (21) being less than about 1:2.

Regarding claims 2, 13 and 15, Tsukamoto does not explicitly disclose the work function ranges of the metal layer formed on the gate dielectric layer as claimed. Chau et al. teach a method of making the metal layer (102), which is formed on the high-k dielectric layer (101), to have different work function ranges that are within the claimed work function ranges (Col. 4, lines 5 to Col. 6, line 14). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Chau et al.'s teachings to Tsukamoto's invention to make the metal layer having a certain work function range as applicant claimed since the way to change the work function of a metal layer is commonly used in the art as disclosed by Chau et al.

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsukamoto (6,040,224 of record) and Chau et al. (6,890,807 of record), as applied to claim 1 above, and further in view of Goto (6,599,819 of record).

Regarding claim 6, the proposed method of Tsukamoto and Chau et al. discloses the claimed invention as detailed above except for specifying the laser beam pulsed at *about 20 nanoseconds or less*.

Although the proposed method of Tsukamoto and Chau et al. does not specify the claimed time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

4. Claims 1-2, 5, 7-8, 10-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2002/0105033 of record) in view of Chau et al. (6,890,807 of record).

Regarding claims 1, 5, 7, 10, and 16, Zhang (see specifically figure 1A) disclose a method of forming a microelectronic structure comprising: providing a substrate (1) comprising source/drain regions (24) and gate region (6/8), wherein the gate region comprises a metal layer (8) disposed on a gate dielectric layer (6) (paragraph [0063]), and laser annealing the substrate to activate the implanted species (paragraph [0071]), wherein the metal layer does not substantially diffuse into the gate dielectric layer (paragraphs [0064]-[0065] and [0072]-[0073]). Zhang fails to teach the gate dielectric layer (6) being a high-k dielectric layer.

Chau et al. while related to a similar method of forming a microelectronic structure teach that the silicon dioxide, which is used to form the gate dielectric layer, is replaced by a high-k

dielectric layer (Col. 1, lines 13+), such as hafnium oxide, zirconium oxide, titanium oxide, and aluminum oxide (Col. 2, lines 32+), in order to reduce gate leakage (Col. 1, lines 14+). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to recognize that combining Chau et al.'s teaching with Zhang's invention would have been beneficial because it helps to reduce gate leakage of the device.

Regarding claims 11 and 14, Chau et al. in the proposed method teach the metal layer can be made of tungsten, which is inherent to have a work function about 4eV, as evidenced by Bustos et al. (U.S. 2004/0126977, paragraph [0067]); and thus, the work function of the metal layer (15) made of tungsten is approximately equal to the work function of a doped polysilicon, as evidenced by Applicant's Specification, paragraph [0018].

Regarding claims 8 and 12, Zhang's figure 1A shows the ratio of the depth of the source/drain regions (24) to the length of the source/drain regions (24) being less than about 1:2.

Regarding claims 2, 13, and 15, Zhang discloses the claimed invention as detailed above except for specifying the work function ranges of the metal layer (e.g., from about 3.9eV to about 5.2eV, from about 3.9eV to about 4.2eV, and from about 4.8eV to about 5.1eV). Chau et al. teach a method of making the metal layer (102), which is formed on the high-k dielectric layer (101), to have different work function ranges that are within the claimed work function ranges (Col. 4, lines 5 to Col. 6, line 14). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply Chau et al.'s teachings to Zhang's invention to make the metal layer having a certain work function range as applicant claimed since the way to change the work function of a metal layer is commonly used in the art as disclosed by Chau et al.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 2002/0105033 of record) and Chau et al. (6,890,807 of record), as applied to claim 1, and further in view of Goto (6,599,819 of record).

Regarding claim 6, the proposed method of Zhang and Chau et al. discloses the claimed invention as detailed above except for specifying the laser beam pulsed at about 20 nanoseconds or less.

Although Zhang and Chau et al. do not specify the time range of the laser beam pulsed (e.g., 20 nanoseconds or less), the annealing time using laser beam is commonly less than 20 ns for activating the implanted regions in a substrate, as disclosed by Goto (Col. 3, lines 49+). It would have been obvious to one of ordinary skill in the art at the time the invention was made to pulse the laser beam to the substrate at about 20 ns or less for activating the implanted regions in the substrate since such the pulsed time of a laser beam is commonly applied in the art, as taught by Goto, and such time range is an art recognized variable of importance which is subject to routine of experimentation and optimization.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luan Thai whose telephone number is 571-272-1935. The examiner can normally be reached on 6:30 AM - 5:00 PM, Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on 571-272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Luan Thai
Primary Examiner
Art Unit 2891
May 26, 2006